REMARKS

This is in response to the Office Action dated March 29, 2005. In that Office Action, Examiner rejected claims 1-18 (all the claims) under 35USC102(e) as being clearly anticipated by Blish, II US Patent 5,914,837. In the Office Action, Examiner noted that: Blish describes an array of voltage regulators (220a-220n) connected in parallel, and having a first voltage regulator that accepts a first power demand that is lower than the second power demands which would be greater. Examiner specifically refers to FIG. 4 of the Blish patent.

Applicants agree with Examiner's characterization of the Blish patent but disagree that it teaches or even suggests applicants' invention. The Blish invention provides a relief to the low voltage, high current spiral trend being seen in the microprocessor industry. A microprocessor module is designed to receive a voltage V2, which is substantially higher than a logic gate utilization voltage V3. Preferably, voltage V2 is substantially greater in magnitude than voltage V3, typically V2:V3 being at least 5:1, but preferably 40:1 to as much as 100:1. (See column 5 lines 31-33.) Since no mention in Blish is made to the contrary, it is presumed that all the regulators provide current to the microprocessor as well as the logic gates at the same speed. None of the regulator circuits are concerned with the speed with which currents are provided because a response to transient events is a problem not addressed in the power supply design of Blish.

In contradistinction, applicants addressed and solved problems of power requirements related to microprocessors and related microelectronic devices that are different from the problem addressed and solved by Blish. In particular, applicants observed that as microprocessor gate counts and clock speeds increase, improved methods and apparatus for supplying not only high current at low voltage but also supplying high current at high speed and low voltage are desired. In this regard, applicants disclose a variety of regulators, in a tiered power regulation system, to

respond to load power demands at different rates. This invention is succinctly claimed, as for example in claim1, as follows:

A tiered power regulation system comprising:

a first power regulator; and

an array comprising a plurality of second power regulators, said second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands,

wherein said array comprising a plurality of second power regulators is configured to couple to a plurality of portions of a microprocessor. (emphasis added)

Thus, while Blish discusses different voltage levels (as demanded in the one case by the microprocessor and in the other case by the logic gates), Applicants' invention provides for a first power regulator (of one type) and a plurality of second power regulators (of another type) configured to respond to a load power demand rate greater than the first power regulator. Applicants' teachings of tiered power regulators responding to differing load power demand rates by the same microprocessor is patentably distinct from the two different power levels provided to the microprocessor and the logic gates by the power regulators of Blish.

Dependent claims 2-8 are believed to be allowable because they depend from an allowable claim and also in that they recite additional features of the invention. For example, there is no teaching in Bliss re: a compound semiconductor substrate (Claim 3).

Regarding claim 7, Blish has no teaching related to the advantages of using discrete electronic components. Regarding claim 8, there is no teaching in Blish to the overall combination with claim 1.

In claim 9, applicants recite:

A tiered power regulation system comprising:

a first power regulator;

a microelectronic device formed on a first substrate; and

an array of second power regulators formed on a second substrate, said second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands. (emphasis added)

As previously noted, there is no teaching in Blish of differently configured power regulators in which the second power regulators respond to a load power demand rate greater than the first power regulators. Dependent claims 10-17 are believed to be allowable for the same reasons and also that they recite additional features of the invention.

Lastly, claim 18 recites:

A tiered power regulation system comprising:

a first power regulator;

a microelectronic device formed on a first substrate; and

an array of second power regulators formed on a second substrate, said second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands,

wherein said array is coupled in parallel to said microelectronic device using bump technology. (emphasis added)

As previously noted, Blish does not teach supplying power to a microelectronic device with second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands. Rather, Blish is limited to different load power demand levels by the microprocessor and logic gates.

In view of the foregoing, it is believed that claims 1-18, all the claims currently in this application, are in condition for allowance. If Examiner has a question or comment or if Applicants' attorney can assist in any manner whatsoever, Examiner is respectfully

requested to telephone the undersigned. An early notification of allowance is earnestly solicited.

Respectfully submitted,
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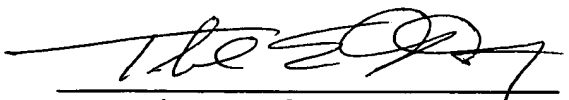

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